

Appl. No. 10/669,111
Reply to Office action of 12/13/2004

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A method of fabricating a depletion drain-extended MOS transistor, comprising:
 - forming a first well of a first conductivity type in a substrate;
 - forming a second well of a second conductivity type in the substrate, the first and second conductivity types being opposite, wherein portions of the first and second wells overlap in a compensated channel region of the substrate;
 - forming a drain of the first conductivity type in a portion of the first well;
 - forming a source of the first conductivity type in a portion of the second well;
 - forming a thick dielectric extending laterally from a first end adjacent the drain to a second opposite end in the first well, the thick dielectric extending into the first well of the substrate;
 - forming a thin dielectric over the substrate, the thin dielectric extending from the second end of the thick dielectric in the first well to the source in the second well, a portion of the thin dielectric extending over the compensated channel region of the substrate; and
 - forming a conductive gate contact structure extending over the thin dielectric and over a portion of the thick dielectric, wherein said compensated channel region is located directly adjacent said source and spaced apart from said thick dielectric.
2. (Original) The method of claim 1, further comprising providing dopants of the second conductivity type in an adjust region of the first well in the substrate proximate the second end of the thick dielectric.

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3. (Original) The method of claim 2, wherein the first well has a concentration of dopants of the first conductivity type less than or equal to a first concentration value proximate the second end of the thick dielectric, and wherein the adjust region has a concentration of dopants of the second conductivity type at a second concentration value in the adjust region, the second concentration value being less than the first concentration value.

4. (Original) The method of claim 2, wherein providing dopants of the second conductivity type in the adjust region comprises implanting dopants of the second conductivity type in the adjust region.

5. (Original) The method of claim 4, wherein implanting dopants of the second conductivity type in the adjust region comprises performing a Vt adjust implant using a Vt adjust mask that exposes the adjust region of the substrate.

6. (Original) The method of claim 4, wherein implanting dopants of the second conductivity type in the adjust region is done after forming the thick dielectric.

7. (Original) The method of claim 2, wherein forming the thick dielectric comprises performing a LOCOS process.

8. (Original) The method of claim 2, wherein forming the thick dielectric comprises performing an STI process.

9. (Original) The method of claim 2, wherein the first conductivity type is n-type and the second conductivity type is p-type.

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10. (Original) The method of claim 2, wherein forming the first well comprises implanting dopants of the first conductivity type into a portion of the substrate using a first well mask exposing the compensated channel region, and wherein forming the second well comprises implanting dopants of the second conductivity type into a portion of the substrate using a second mask exposing the compensated channel region.

11. (Original) The method of claim 10, wherein dopants of the first conductivity type are implanted using the first mask at a first implantation dose, wherein dopants of the second conductivity type are implanted using the second mask at a second implantation dose, and wherein the first dose is greater than or equal to the second dose.

12. (Original) The method of claim 11, wherein the first conductivity type is n-type and the second conductivity type is p-type.

13. (Currently Amended) A method of fabricating a depletion drain-extended MOS transistor, comprising:

forming a source and a drain in a substrate, the source and drain being of a first conductivity type;

forming a gate structure over a channel region of the substrate, the gate structure comprising:

a thick dielectric having a first end adjacent the drain and extending laterally toward the source to a second opposite end, the thick dielectric extending into the substrate;

a thin dielectric extending over the substrate from the second end of the thick dielectric to the source; and

a conductive gate contact structure extending over the thin dielectric and over a portion of the thick dielectric;

forming a compensated channel region extending below a portion of the thin dielectric in the substrate adjacent and physically contacting the source, the

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compensated channel region comprising dopants of the first and second conductivity types; and

forming an adjust region in the substrate proximate the second end of the thick dielectric, the adjust region comprising dopants of the second conductivity type and being spaced apart from said compensated channel region.

14. (Original) The method of claim 13, wherein providing dopants of the second conductivity type in the adjust region comprises implanting dopants of the second conductivity type in the adjust region.

15. (Original) The method of claim 14, wherein implanting dopants of the second conductivity type in the adjust region comprises performing a Vt adjust implant using a Vt adjust mask that exposes the adjust region of the substrate.

16. (Original) The method of claim 13, wherein the first conductivity type is n-type and the second conductivity type is p-type.

17. (Original) The method of claim 13, wherein forming a compensated channel region comprises:

implanting dopants of the first conductivity type into a portion of the substrate using a first well mask exposing the compensated channel region; and

implanting dopants of the second conductivity type into a portion of the substrate using a second mask exposing the compensated channel region.

18. (Original) The method of claim 17, wherein dopants of the first conductivity type are implanted using the first mask at a first implantation dose, wherein dopants of the second conductivity type are implanted using the second mask at a second implantation dose, and wherein the first dose is greater than or equal to the second dose.

Claims 19-26 (canceled).